Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended and new claims added to more clearly claim Applicants invention and overcome Examiners rejections. Support for the amended and newly drafted claims are found in the original claims and/or Specification. For example, support for amendments in claims 1, 15, 20 and new claim 21 is found in the following Specification excerpts at paragraphs 0023 and 0024:

"As shown in Figure 2B, in the method according to the present invention, the exposed hard mask region 32 is anisotropically etched through to the polysilicon layer 26 to form the outline of a gate structure. Following, the plasma etching step, **the photoresist is stripped (removed) according to a conventional ashing or wet chemical process to leave hard mask layer 28 overlying the polysilicon layer 26** and outlining the upper portion of a gate structure.

According to one embodiment of the present invention, a semiconductor wafer including the patterned hard mask layer 28 **is subjected to an isotropic wet etching process to isotropically trim down the hard mask layer 28 to form a reduced dimension portion 34** outlining a gate structure as shown in Figure 2C. The hard mask layer 28 is reduced in dimension for example, **including reducing a width of the gate structure from about 100 nm to between about 10 nm to about 50 nm**, more preferably to about 30 nm, as shown in Figure 2C, the

width dimension being indicated by dimensional arrow 35. Preferably the isotropic wet etching process is carried out by placing the wafer on a conventional spin chuck as used in a single wafer spray etching process. It will be appreciated that the wet etching process according to the present invention may use any conventional wet etching process, for example immersion or spraying. **A spraying process, for example, using a single wafer spinning chuck to spin the semiconductor wafer while simultaneously spraying the semiconductor etching surface with a source of etching solution is preferred since it has been found to give superior etching uniformity and control of critical dimension (CD) bias across a semiconductor wafer surface.**

Following the isotropic wet etching process to reduce dimension of a hard mask defining a semiconductor feature dimension, for example, a gate structure width, **a conventional anisotropic plasma etching procedure** may be carried out on the exposed portions of the semiconductor wafer substrate (areas not covered by the hard mask layer 28) to complete the formation of the semiconductor feature, for example, a gate structure, as shown in Figure 2D."

Support for new claim 24 is found in the following Specification excerpt at paragraph 0029:

"Optionally, the spraying (spin-spray) etching procedure according to the present invention may be carried out in more than one step, for example, altering the parameters including etching solution concentration and spin rate to achieve faster etch rates over a portion of the etching dimension, **followed by a more mild etching solution concentration with a slower etch rate as critical dimension limits are approached.**"

The remaining amendments and newly drafted claims find support in the original claims and/or the Specification. No new matter has been entered.

Claim Rejections under 35 USC 112

Claim 15 has been amended to overcome Examiners rejection.

Claim Rejections under 35 USC 102(e)

1. Claims 1, 2, 4-6, 15 stand rejected under 35 USC 102(e) as being anticipated by Pike et al. (US 6,420,097).

Pike et al. disclose a method for trimming a hardmask layer to overcome the problem of simultaneous resist trimming during trimming the hardmask layer (see e.g., Abstract, col 2, lines 43-45, col 3, lines 33-35).

Pike et al. teach leaving the resist over the hardmask during the trimming process to prevent material loss from the top of the hardmask during a **lateral** trimming process (col 4, lines 25-29) which is not an **isotropic** trimming process thereby failing to anticipate Applicants amended claims 1 and 15, but rather specifically teaching away therefrom.

Pike et al. further fail to disclose or teach a specific etch process or etch chemistry.

Pike et al. clearly fail to anticipate Applicants disclosed and claimed invention, but rather specifically teaches away therefrom.

2. Claims 1, 2, 4-6, 15 stand rejected under 35 USC 102(b) as being anticipated by McKee (US 5,804,088).

McKee discloses laterally etching either an overlying photoresist etch and/or an underlying layer and specifically where an underlying BARC is selectively **laterally** etched (trimmed) (col 1, lines 66) to reduce a width compared to the overlying photoresist layer (e.g., see Fig 8d) which is left in place preventing **isotropic** trimming. The underlying layer is disclosed to be an ARC layer, an etchstop, sacrificial layer, and/or a liftoff layer. Similar to Pike et al., the method of McKee leaves the overlying photoresist layer in place during etching of the underlying layer (e.g., hardmask) (col 3, lines 33-45) and although referred to as an "isotropic" etch is not an **isotropic trimming** process since the remaining photoresist protects etching of the upper surface.

McKee discloses the use of organic and TiN BARC layers as an underlying layer (e.g., hard mask). McKee discloses an 'isotropic' dry etch process (col 4, lines 22-44) to etch both the resist and underlying organic BARC layers and a wet 'isotropic' etch including H_2O_2 to selectively **laterally etch** TiN with the top portion protected by overlying photoresist (col 5, lines 59-67, Fig 8D). McKee does not disclose the use of silicon nitride or silicon oxynitride as a hardmask, or a specific wet etching process (e.g., immersion or spin/spray).

McKee clearly fails to anticipate Applicants disclosed and claimed invention, but rather specifically teaches away therefrom.

Claim Rejections under 35 USC 103(a)

3. Claims 3 and 20 stand rejected under 35 USC 103(a) as being unpatentable over Pike et al., above.

Applicants repeat the arguments and assertions made with respect to Pike et al. above. Moreover, Applicants point out that neither Pike et al. nor McKee recognize, solve, or suggest a solution to the problem that Applicants have recognized and solved by their claimed invention:

"A method for **isotropically** trimming semiconductor feature sizes with improved critical dimension uniformity across a process wafer surface"

The methods of both Pike et al. and McKee operate by a different principal of operation where a photoresist layer protects the hardmask during the 'isotropic' etching process thereby **not** resulting in **isotropically reduced** hardmask dimensions as disclosed and claimed by Applicants. Moreover there is no teaching or suggestion that a spin/spray process would be successful when leaving a resist layer overlying the hardmask.

Further, neither Pike et al. nor McKee disclose the isotropic trimming processes claimed by Applicants.

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).*

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc.,*

721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).

Moreover, Examiners argument of "routine experimentation" clearly fails since it is well settled that to make out a *prima facie* case of obviousness the general conditions of Applicants claimed invention must first be shown, on which point Pike et al. and McKee et al. fail.

"A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation." *In re Antonie*, 559 F.2d 618, 195 USPQ 6 (CCPA 1977).

3. Claims 3 and 20 stand rejected under 35 USC 103(a) as being unpatentable over McKee, above and further in view of Pike et al.

Applicants reiterate the statements made above with respect to Pike et al. and McKee.

4. Claims 7-9, 14, 17 stand rejected under 35 USC 103(a) as being unpatentable over Pike et al. or Pike et al. and McKee, as

applied to claims 1 and 15 and further in view of admitted prior art.

Applicants reiterate the statements made above with respect to Pike et al. and McKee.

Applicants reproduce a relevant portion of the Specification in the detailed description to which Examiner is apparently referring to in citing Applicants admitted prior art:

"It will be appreciated that the wet etching process according to the present invention may use **any conventional wet etching process, for example immersion or spraying**. **A spraying process**, for example, using a single wafer spinning chuck to spin the semiconductor wafer while simultaneously spraying the semiconductor etching surface with a source of etching solution **is preferred since it has been found to give superior etching uniformity and control of critical dimension (CD) bias across a semiconductor wafer surface.**"

Examiner is improperly referring to Applicants disclosure to find both the elements of Applicants claimed invention and motivation to modify Pike et al. and/or McKee.

"First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must

be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. **The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.**" *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Even conceding *arguendo* that a spin/spray etching process or etching with phosphorous acid is well known does not help Examiner in establishing a *prima facie* case.

First, Applicants respectfully point out that Examiner misstates the teachings of Applicants disclosure by arguing that it would have been obvious "to etch metal nitride **by immersion or spray etching** using phosphorous acid at 150 to 180 °C". Applicants do not teach or claim spray etching with phosphorous acid.

Secondly, the fact that individual aspects of Applicants invention are well known does not help Examiner in establishing a *prima facie* case of obviousness.

"The fact that references relied upon teach that all aspects of the claimed invention were individually known in the art is

not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)*.

5. Claims 10-13, 18, and 19 stand rejected under 35 USC 103(a) as being unpatentable over Pike et al. as applied to claims 1 and 15 and further in view of Decker et al. (US 4,269,654).

Decker et al. disclose an etching solution for etching composite structures of silicon nitride and silicon oxide (see Abstract) to produce tapered openings (see col 2, lines 62-69 - col 3, lines 1-3). Decker et al. discloses the use of "glycerol, ethers such as ethylene glycol monoethyl ether, ethylene glycol, and the like" (col 3, lines 19-21) together with HF. Decker et al. disclose an etching temperature between about 80 °C and 115 °C (col 3, lines 26-27). Decker et al. teach an etching process including **leaving an overlying resist layer in place** to protect the surface col 3, lines 30-35) and teaches away from etching below a temperature of 75 °C (col 3, line 36).

Decker et al. do not disclose or suggest a process for trimming a hardmask layer either laterally or isotropically, nor disclose or teach an isotropic etching process not suggest the

desirability of using the etchant for silicon oxynitride or titanium nitride or suggest its usefulness in trimming a hardmask layer. There is no apparent motivation for combining Decker et al. with Pike et al. or McKee since Decker et al. teach forming a tapered opening while Pike et al. or McKee teach **laterally trimming** a hardmask layer to achieve critical dimensions. However, even assuming *arguendo* proper motivation for such combination, such combination does not produce Applicants claimed invention as shown above with respect to Pike et al. or McKee.

Moreover, Decker et al. do not recognizes, suggest or solve the problem that Applicants have recognized and solved by their disclosed and claimed invention, but rather specifically teaches away from Applicants claimed invention by teaching a temperature range above the range disclosed and claimed by Applicants and teaching leaving a resist layer overlying the etching surface. Further, Decker et al. specifically teach away from the use of phosphoric acid due to the problem of undercutting the overlying resist layer (col 1, lines 45-50).

With respect to the independent claims, since the teachings of Pike et al., McKee, Decker et al., or Applicants admitted prior art, or any combination thereof, fail to produce Applicants claimed invention, thereby failing to make out a *prima facie* case

of obviousness sufficient under 35 USC 103(a) with respect to the amended independent claims 1 and 15, neither has a *prima facie* case of obviousness been made out with respect to the amended and newly drafted dependent claims.

The Claims have been amended to clarify Applicants claimed invention and newly drafted claims added. A favorable consideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited. The Commissioner is hereby authorized to charge Deposit Account No. 50-0484 any fee due as a result of this response.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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